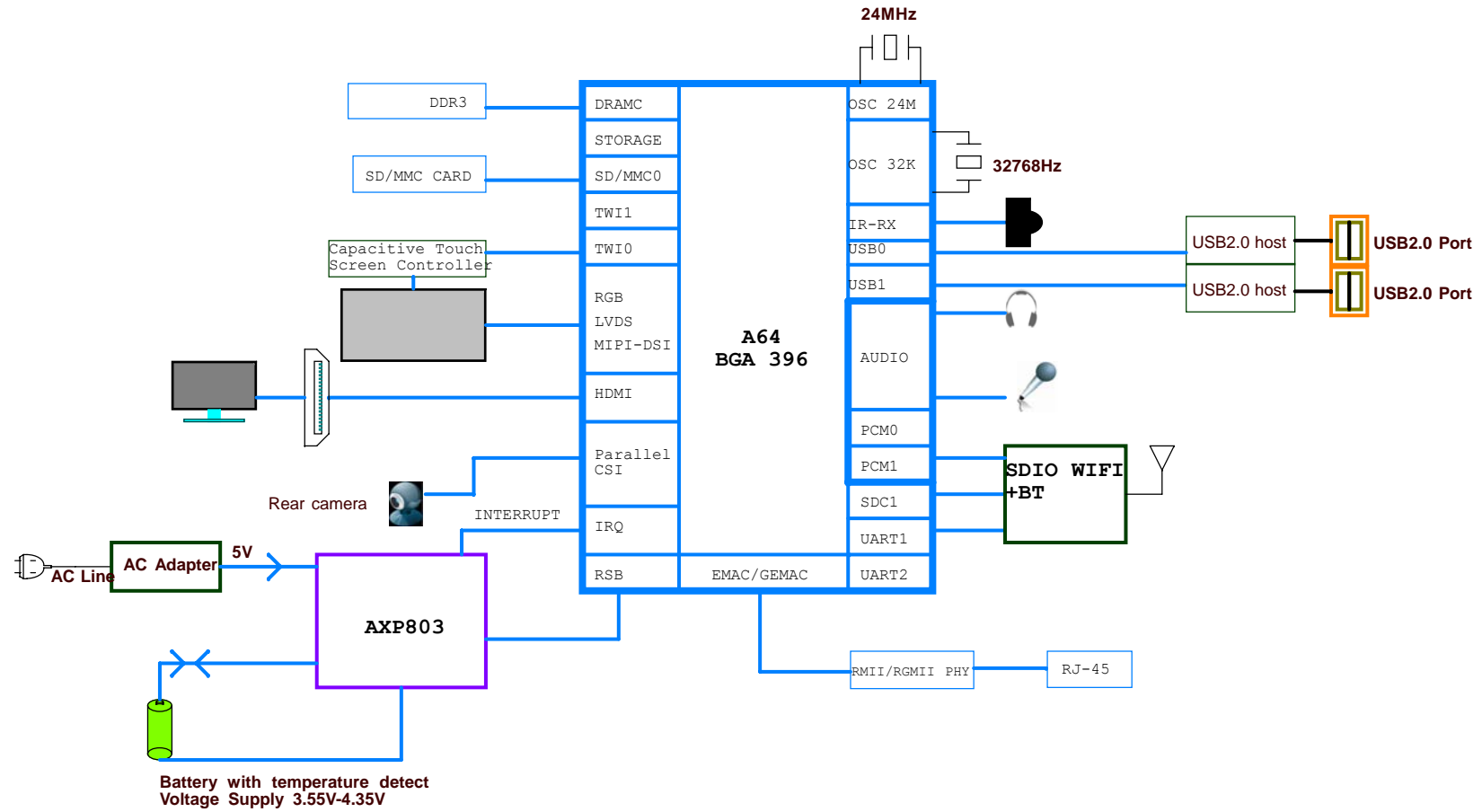
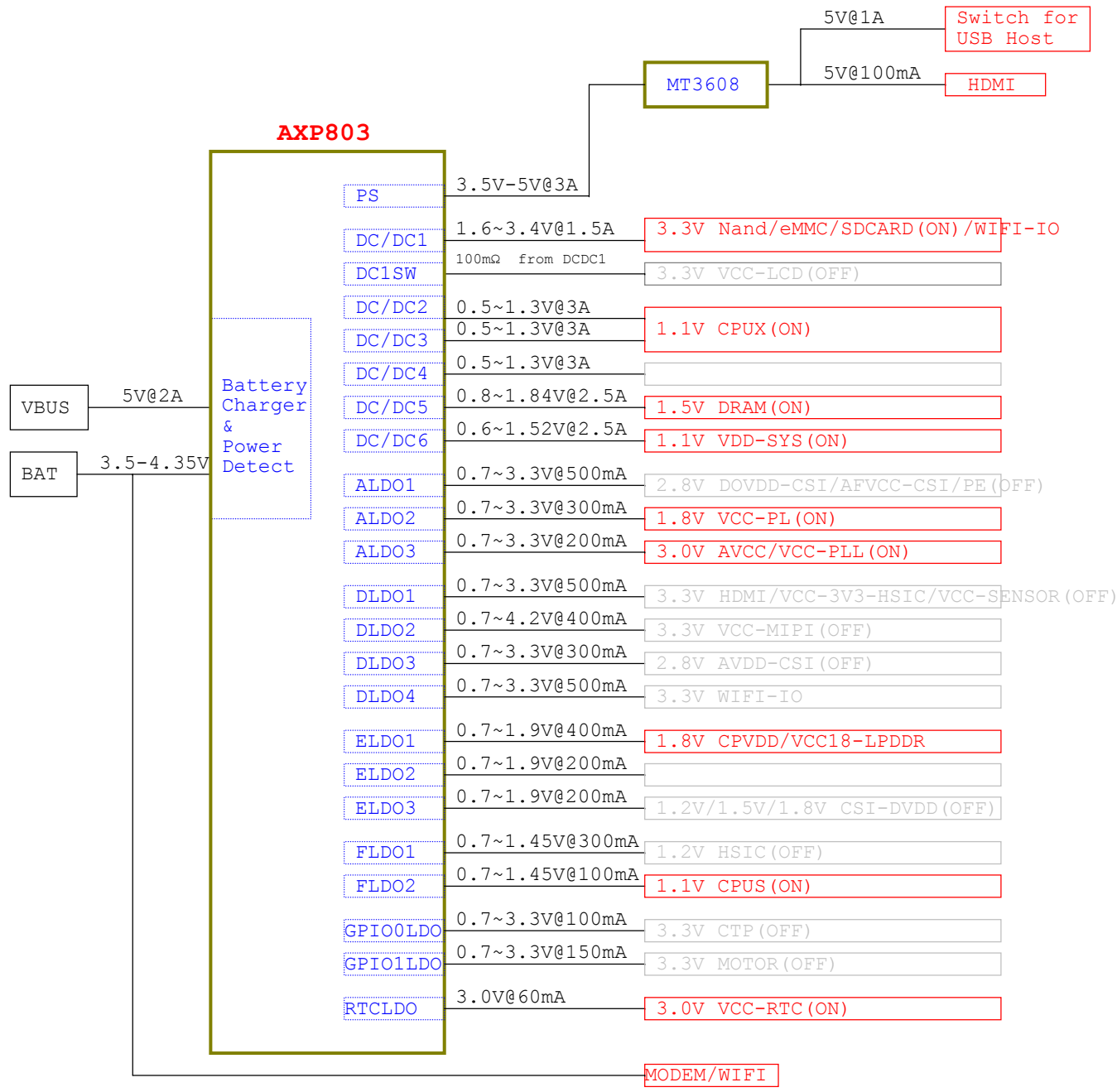


BLOCK DIAGRAM



PINE64			
Title SOPINE Baseboard " Model A"			
Size A3	Document Number BLOCK DIAGRAM	Rev 0.9	
Date:	Sheet 2 of 19		1

POWER TREE



PINE64			
Title SOPINE Baseboard " Model A"			
Size A3	Document Number	POWER TREE	Rev 0.9
Date:	Sheet 3 of 19		

LPDDR3 32X1

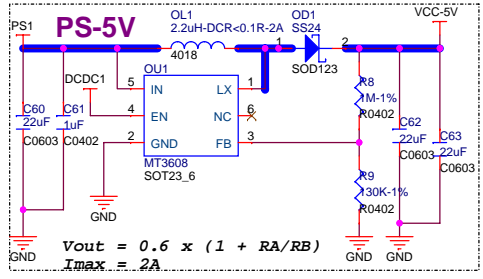
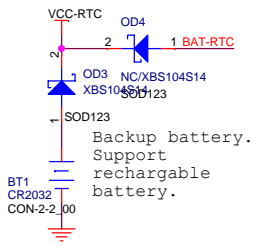
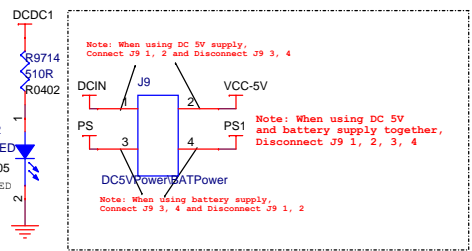
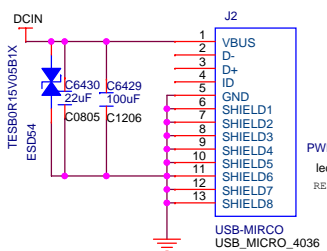


PINE64		
Title SOPINE Baseboard " Model A"		
Size A3	Document Number DDR3 16X2	Rev 0.9
Date:	Sheet 4 of 19	

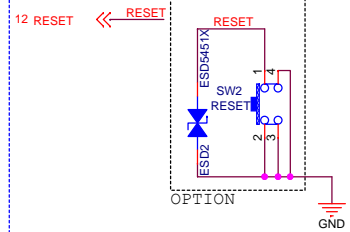
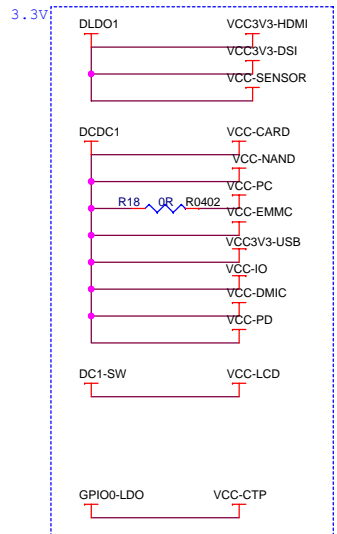
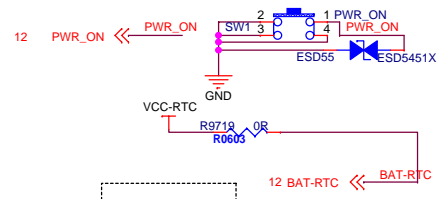
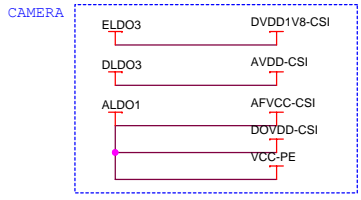
CPU

PINE64		
Title SOPINE Baseboard " Model A"		
Size A3	Document Number CPU	Rev 0.9
Date:	Sheet 5 of 19	

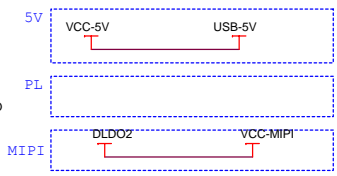
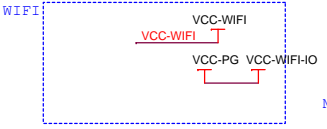
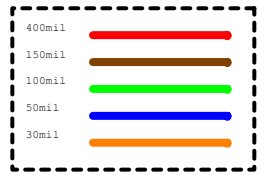
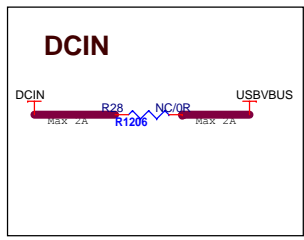
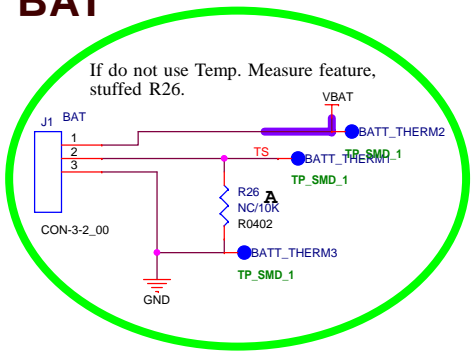
Power



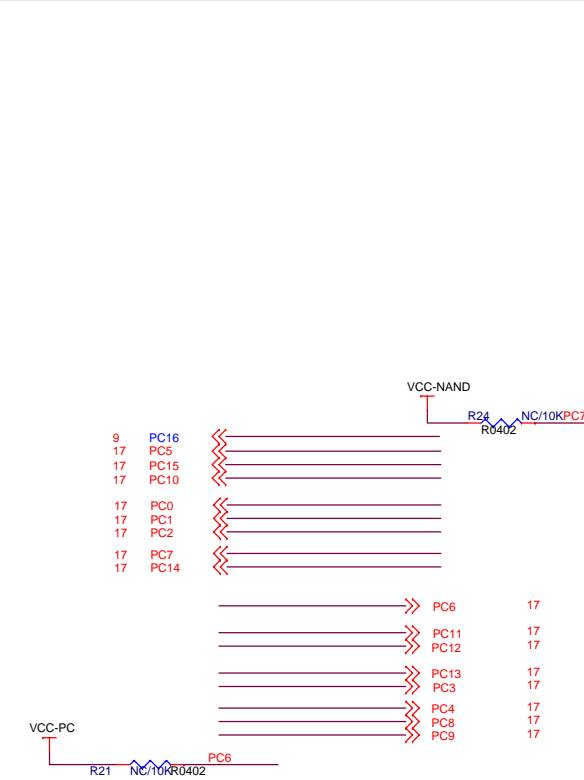
12 TS ← TS
12 CHGLED ← CHGLED



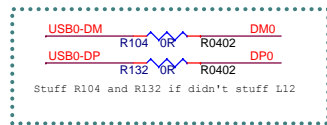
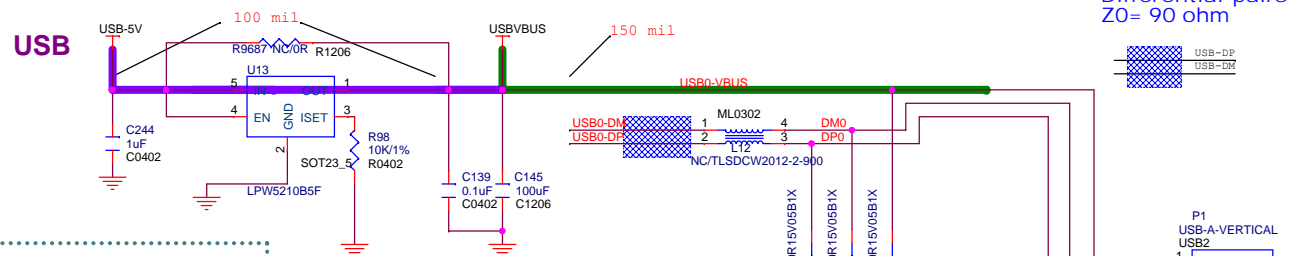
Lithium BAT



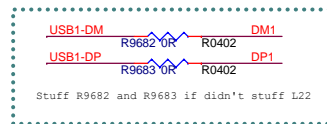
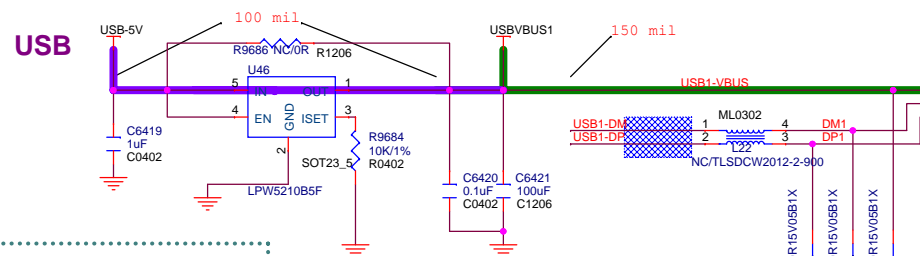
PINE64			
Title SOPINE Baseboard " Model A"			
Size A3	Document Number	PMIC	Rev 0.9
Date:	Sheet 6 of 19		



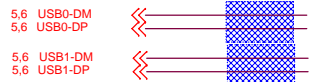
PINE64			
Title SOPINE Baseboard " Model A"			
Size A3	Document Number EMMC		Rev 0.9
Date:	Sheet 7 of 19		



The ESD part's parasitic capacitance < 5pF.

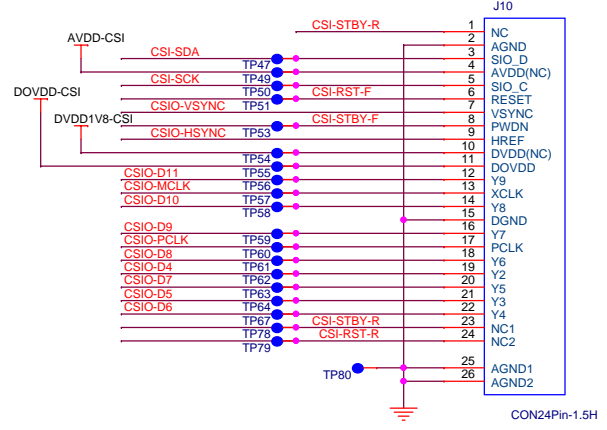
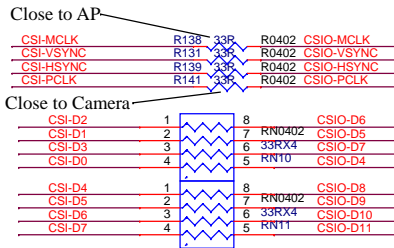
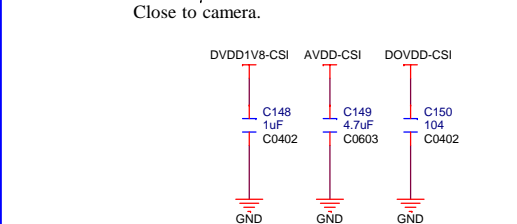
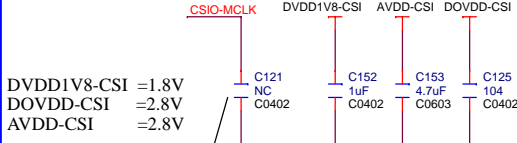
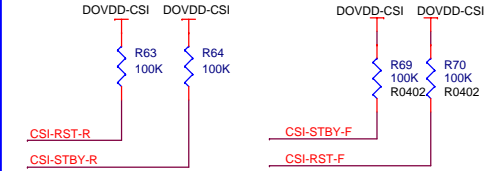
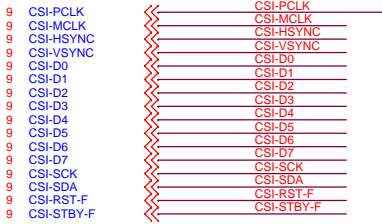
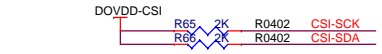


The ESD part's parasitic capacitance < 5pF.

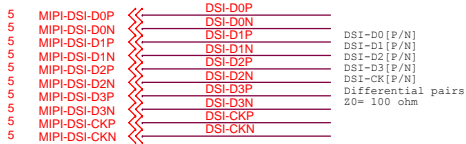
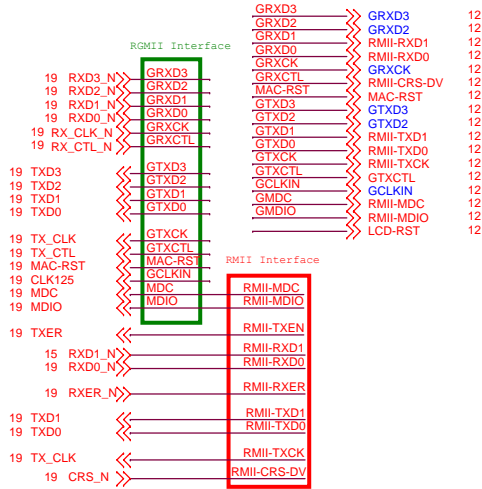
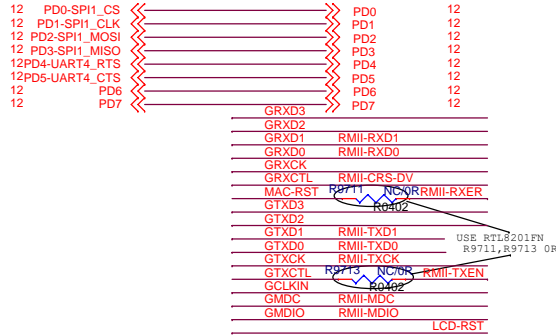


PINE64		
Title SOPINE Baseboard " Model A"		
Size A3	Document Number	Rev 0.9
Date:		USB/T-CARD
Sheet 9		of 19

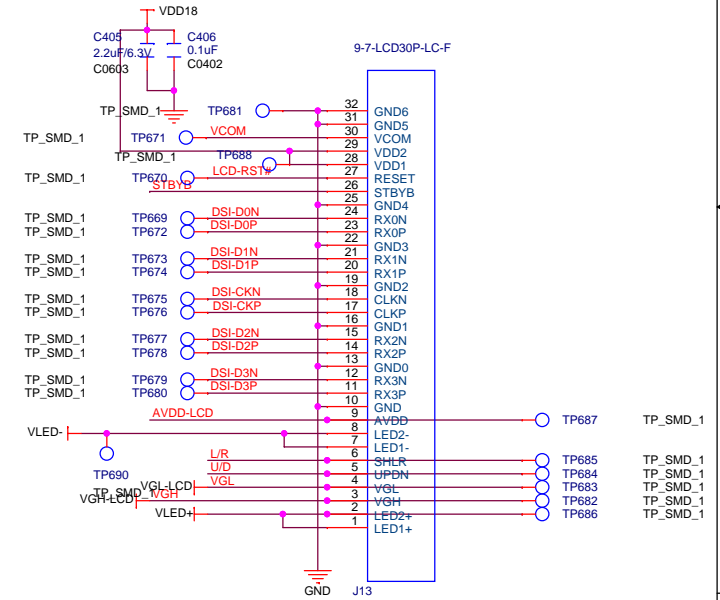
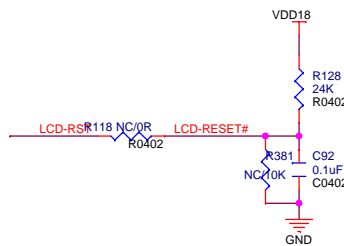
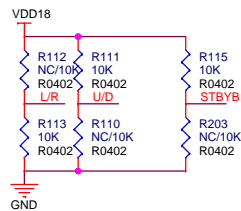
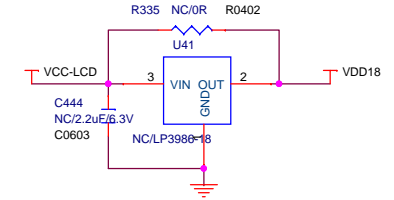
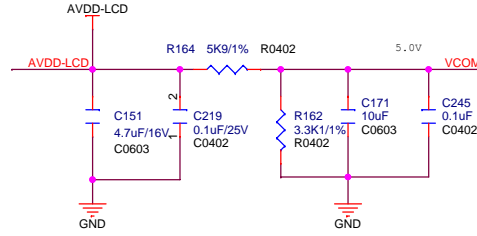
CAMERA



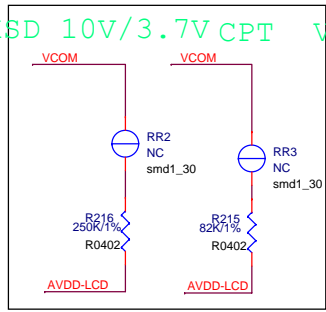
LCD



MIPI-LCD

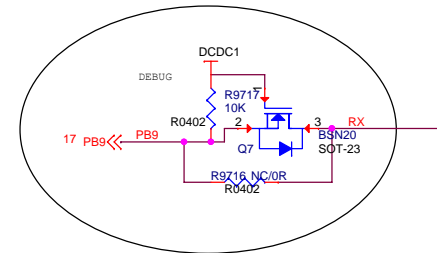
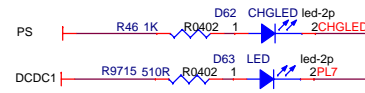
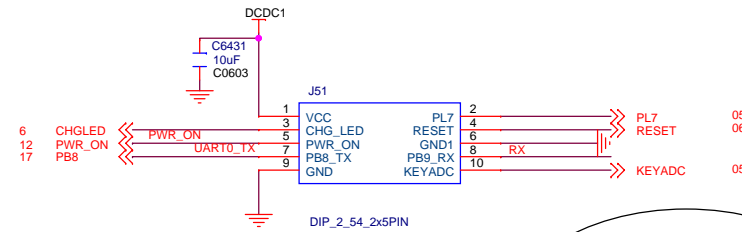
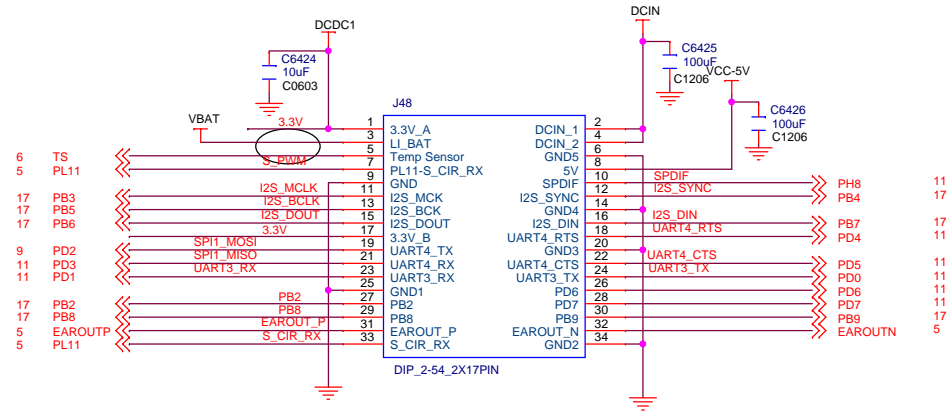


HSD 10V/3.7V CPT Vcom=4.3V



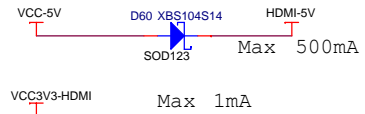
PINE64		
Title SOPINE Baseboard " Model A "		
Size A3	Document Number LCD	Rev 0.9
Date:	Sheet 11	of 19

Euler bus

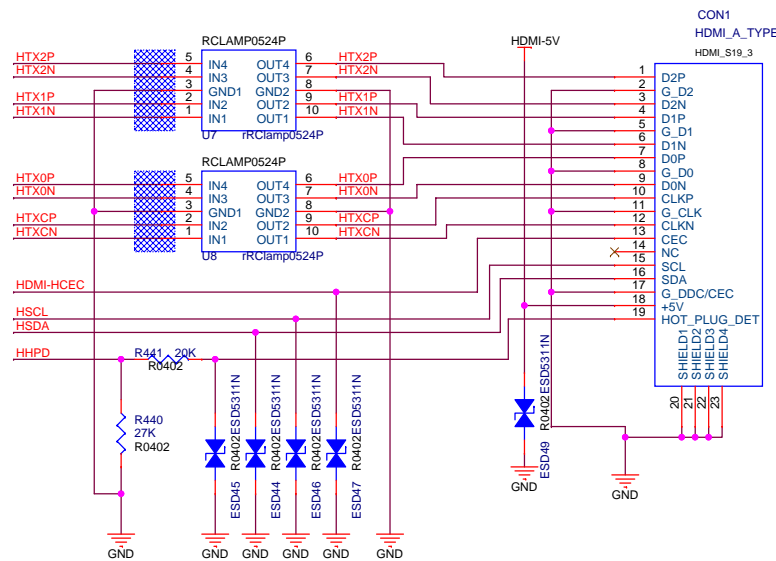
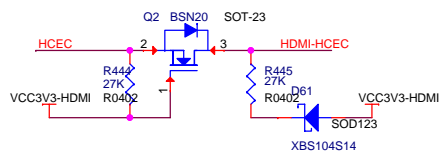
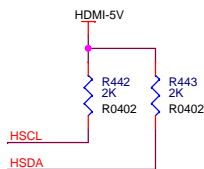


PINE64		
Title SOPINE Baseboard " Model A"		
Size A3	Document Number Euler e Connector	Rev 0.9
Date:	Sheet 12 of 19	

HDMI

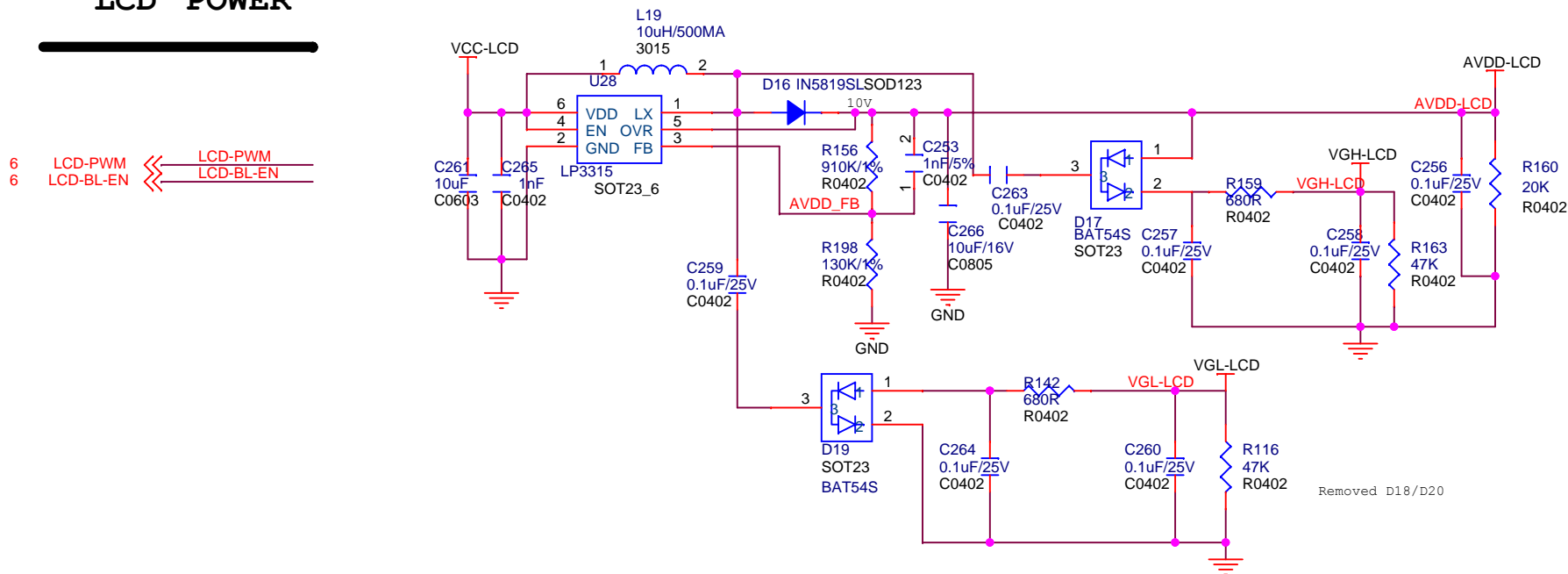


Differential pairs
Z0= 100 ohm

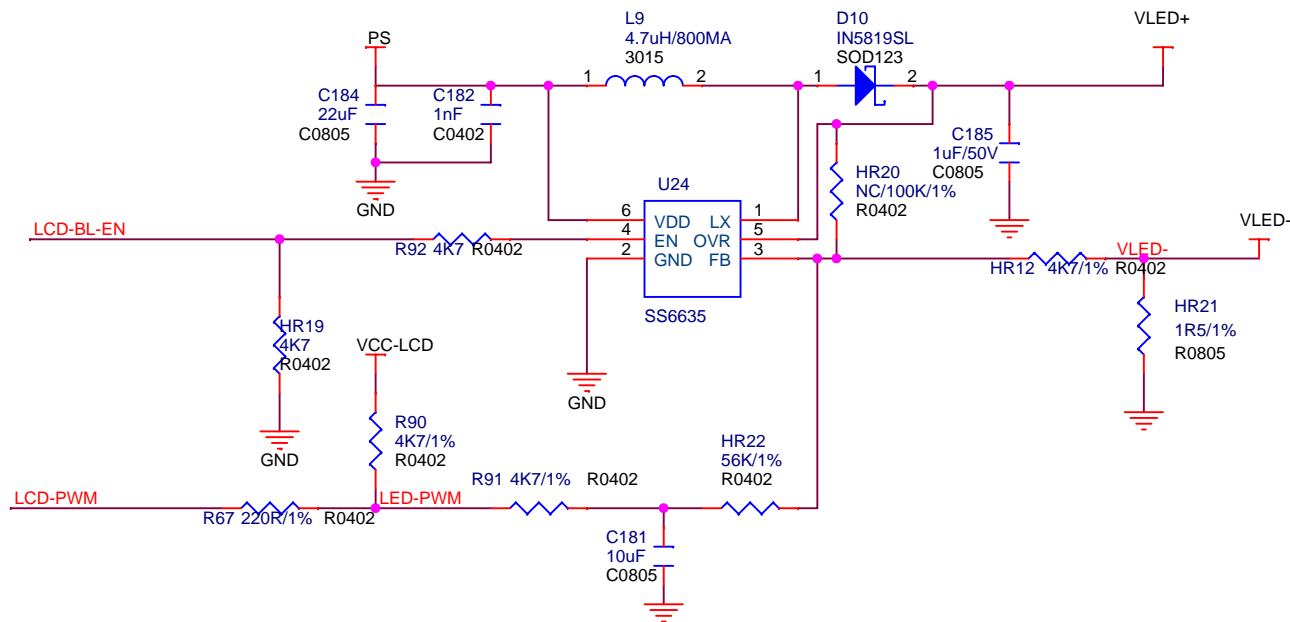


PINE64		
Title SOPINE Baseboard " Model A"		
Size A3	Document Number HDMI	Rev 0.9
Date:	Sheet 13 of 19	

LCD POWER



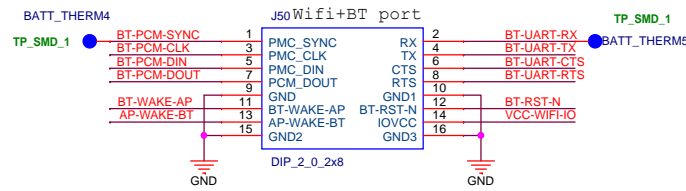
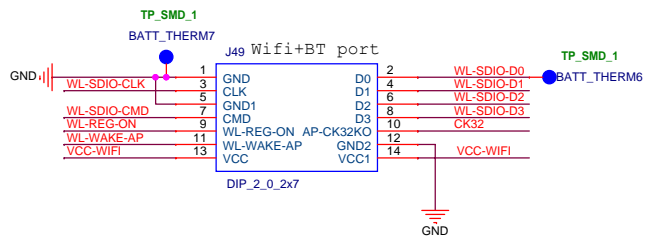
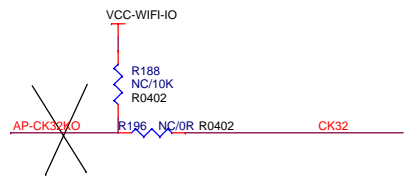
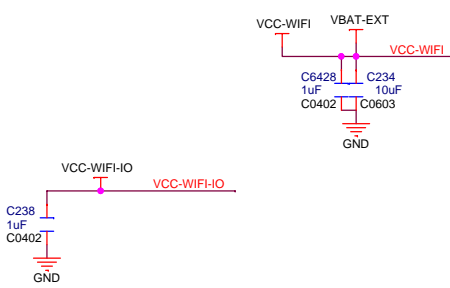
Backlight



PINE64

Title		
SOPINE Baseboard " Model A"		
Size	Document Number	Rev
A4	LED POWER	0.9
Date:	Sheet	14 of 19

- | | | |
|---|-------------|-------------|
| 9 | WL-SDIO-CLK | WL-SDIO-CLK |
| 9 | WL-SDIO-CMD | WL-SDIO-CMD |
| 9 | WL-SDIO-D0 | WL-SDIO-D0 |
| 9 | WL-SDIO-D1 | WL-SDIO-D1 |
| 9 | WL-SDIO-D2 | WL-SDIO-D2 |
| 9 | WL-SDIO-D3 | WL-SDIO-D3 |
| 9 | BT-UART-RX | BT-UART-RX |
| 9 | BT-UART-TX | BT-UART-TX |
| 9 | BT-UART-CTS | BT-UART-CTS |
| 9 | BT-UART-RTS | BT-UART-RTS |
| 9 | BT-PCM-SYNC | BT-PCM-SYNC |
| 9 | BT-PCM-CLK | BT-PCM-CLK |
| 9 | BT-PCM-DIN | BT-PCM-DIN |
| 9 | BT-PCM-DOUT | BT-PCM-DOUT |
| | | |
| 9 | WL-PMU-EN | WL-REG-ON |
| 9 | WL-WAKE-AP | WL-WAKE-AP |
| 9 | BT-WAKE-AP | BT-WAKE-AP |
| 9 | BT-RST-N | BT-RST-N |
| 9 | AP-WAKE-BT | AP-WAKE-BT |

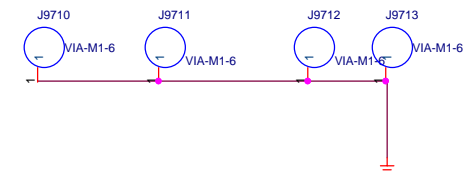
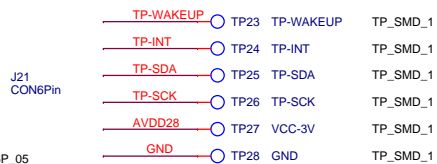
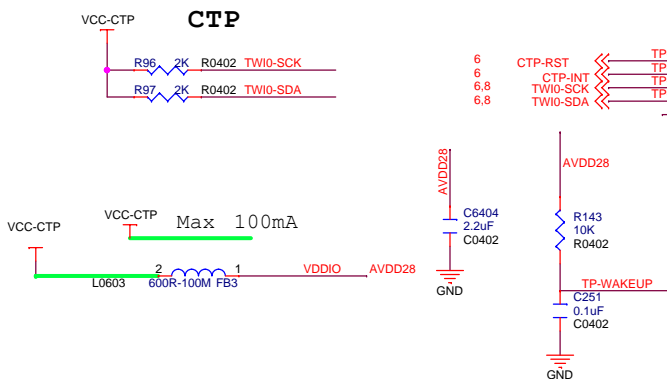
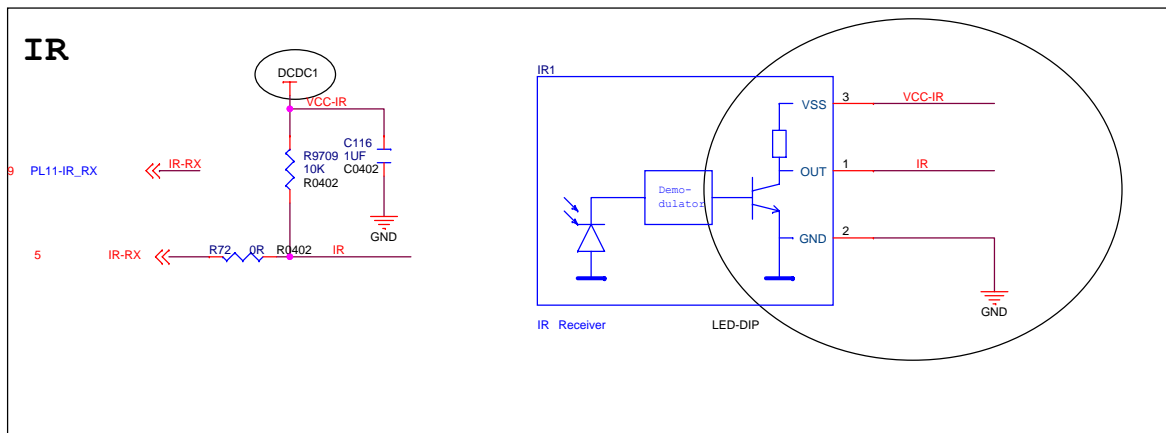


VCC-WIFI-HO

PINE64			
Title SOPINE Baseboard " Model A"			
Size A3	Document Number	WIFI+BT	Rev 0.9
Date:	Sheet 15 of 19		

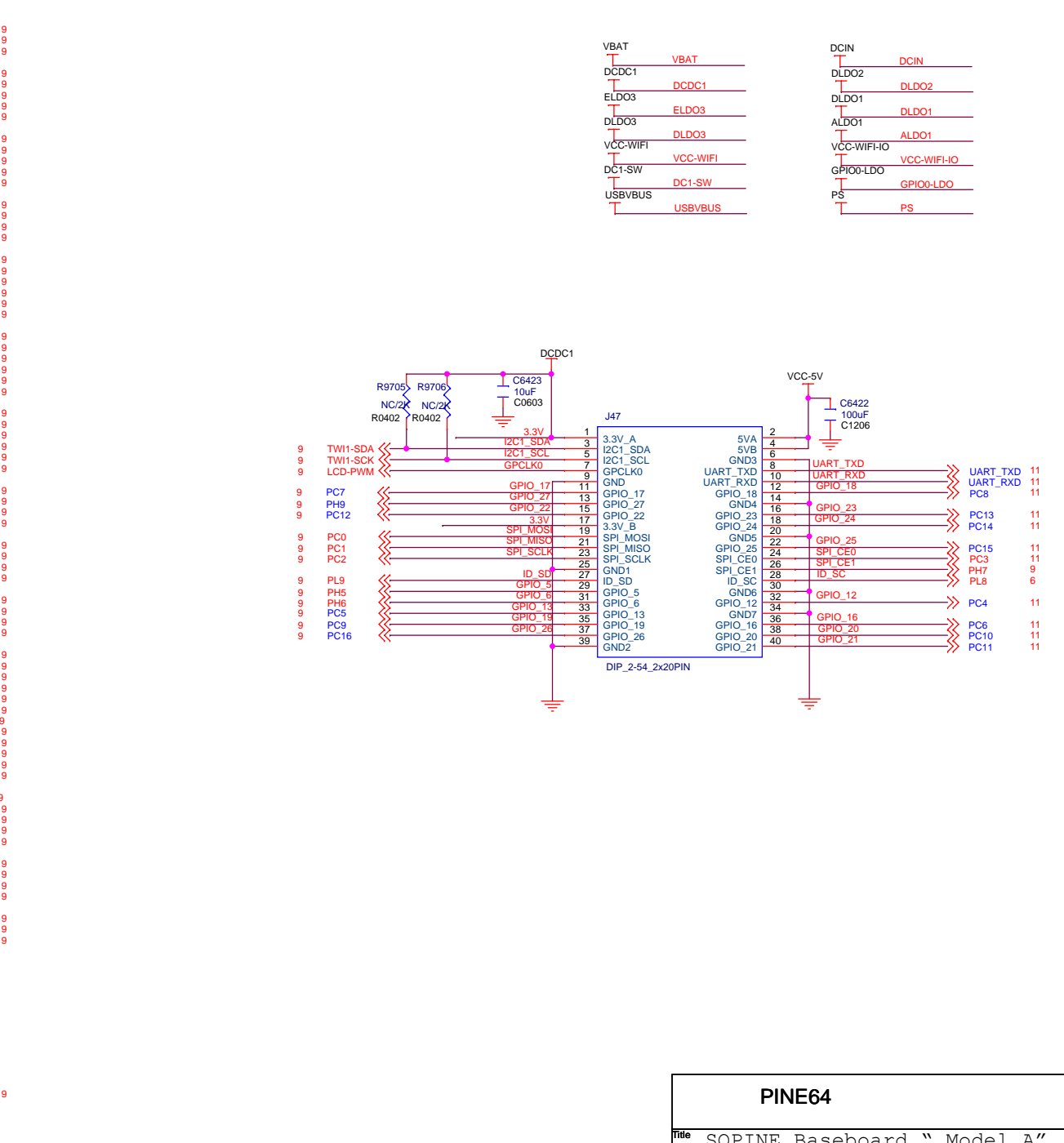
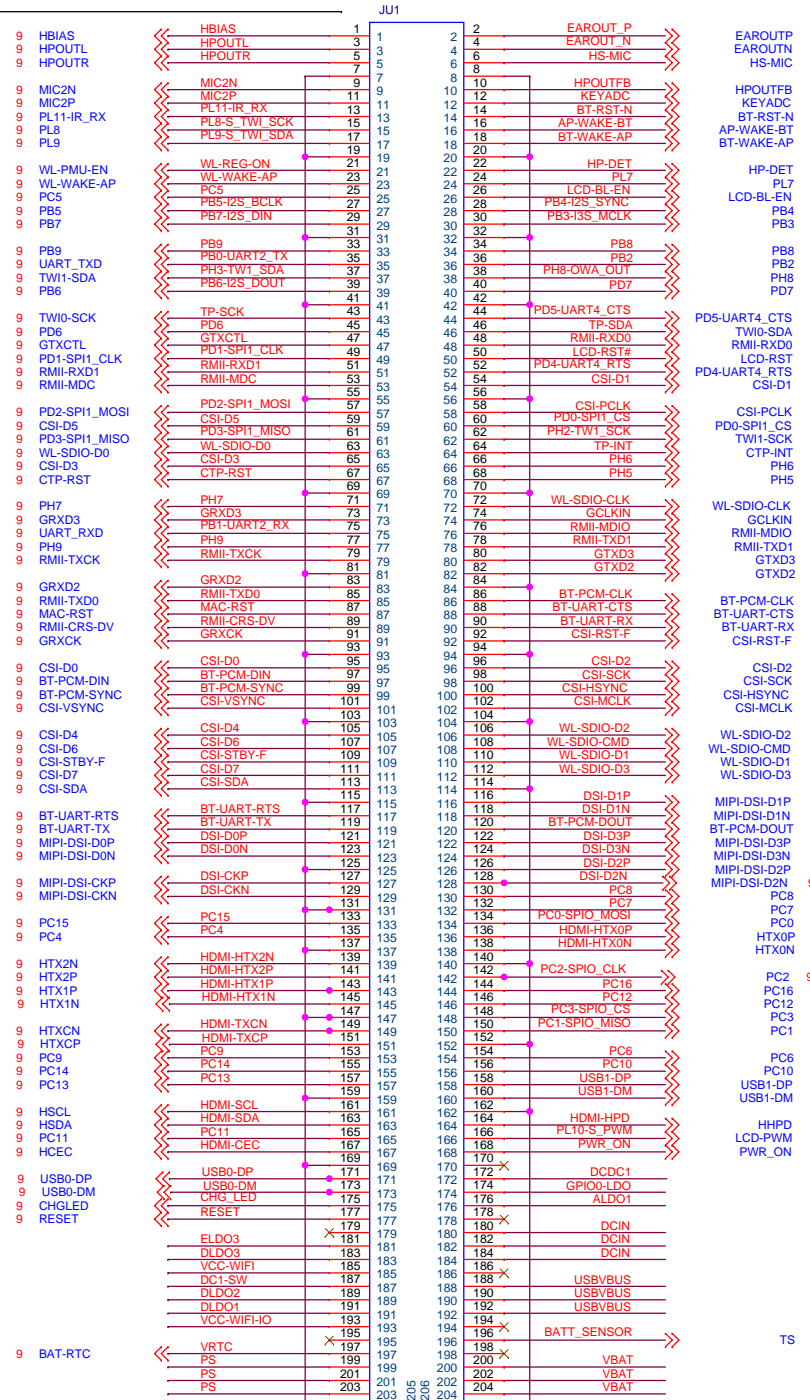
CTP

IR



PINE64		
Title SOPINE Baseboard " Model A"		
Size A3	Document Number CTP/IR	Rev 0.9
Date:	Sheet 16	of 19

PI-2 bus

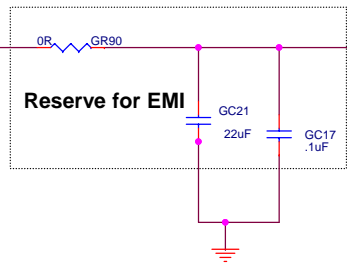


PINE64

Title SOPINE Baseboard " Model A"

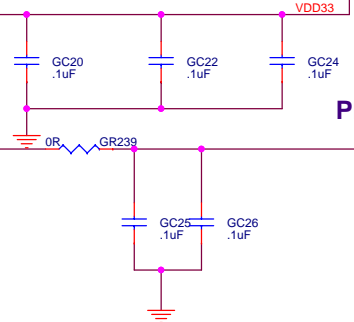
Size A3	Document Number Pi-2 Connector	Rev 0.9
Date:	Sheet 17 of 19	

GMAC-3V



PHY_VDD33

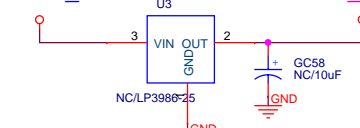
PHY_AVDD33



3.3/2.5V RGMII Power

PHY_VDD33

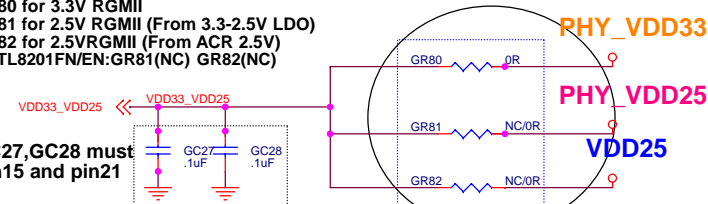
PHY_VDD25



Reserve for 2.5V RGMII power (if MAC support 2.5V RGMII)

R80 for 3.3V RGMII
R81 for 2.5V RGMII (From 3.3-2.5V LDO)
R82 for 2.5VRGMII (From ACR 2.5V)
RTL8201FN/EN:GR81(NC) GR82(NC)

For EMI GC27,GC28 must close to pin15 and pin21



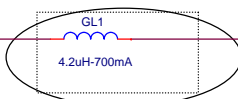
RTL8211CN/D/E	GL1	C56	U10	GR65	GR66	GR122	GC41/GC57
Enable switching regulator	○	○	✗	○	✗	✗	○
Disable switching regulator	✗	✗	○	✗	○	○	✗

Note 1: The Trace length between GL1 and Pin 48 must be within 0.5 cm. GC40 and GC41 to G L1 must be within 0.5cm.

RTL8211D/8211CN:GC40 22uF(X5R)
RTL8211E: GC40 4.7uF(X5R)

GMAC-3V

REGOUT

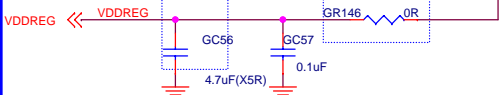


RTL8211D/8211CN: L1=4.7uH
RTL8211E: L1= 2.2uH

VDDREG

PHY_AVDD33

Note 2: The Trace length from C56, C57 to Pin 44,45 must be within 1 cm. The trace width from PHY_AVDD33 to Pin 44,45 should >40mils

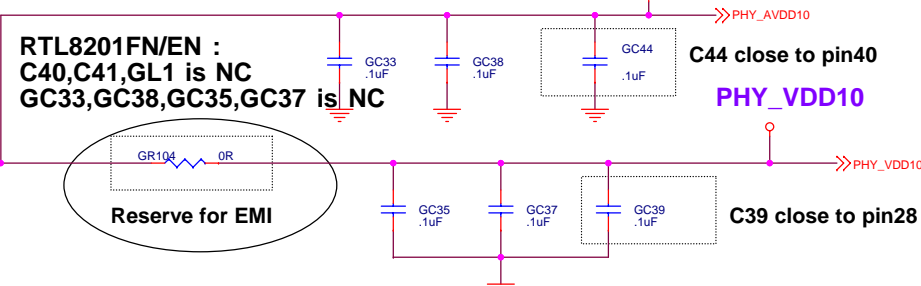


Isolation VDDREG and AVDD33
RTL8201FN/EN:GC56(NC),GC57(NC),GR146(NC)
RTL8211CN/8211D: GC56 22uF(X5R)
RTL8211E: GC56 4.7uF(X5R)

External Power Source

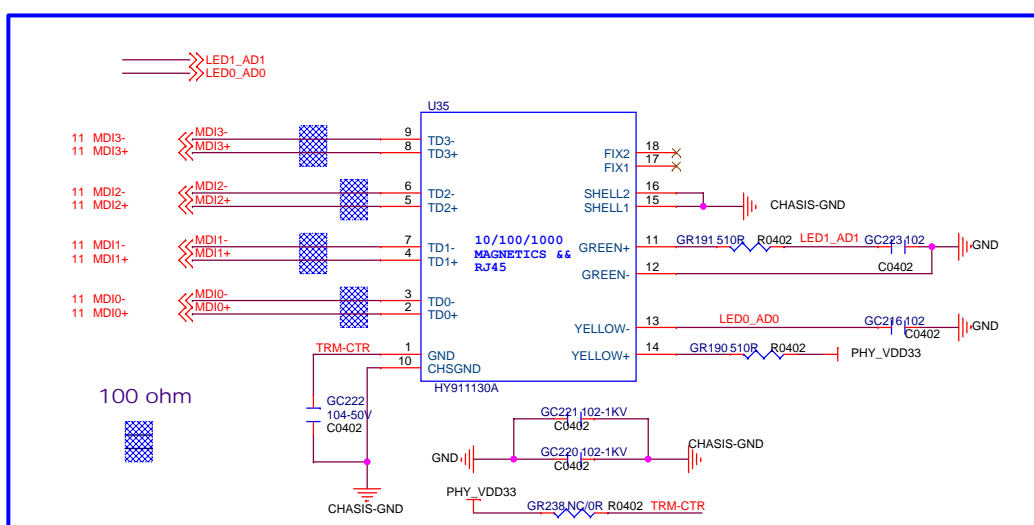
U10,GC69,GC68, GR122,GR120 and GR121 are only used by 8211CN/8211D/8211E application when switching regulator is disabled. For other applications, please remove them.

RESERVE

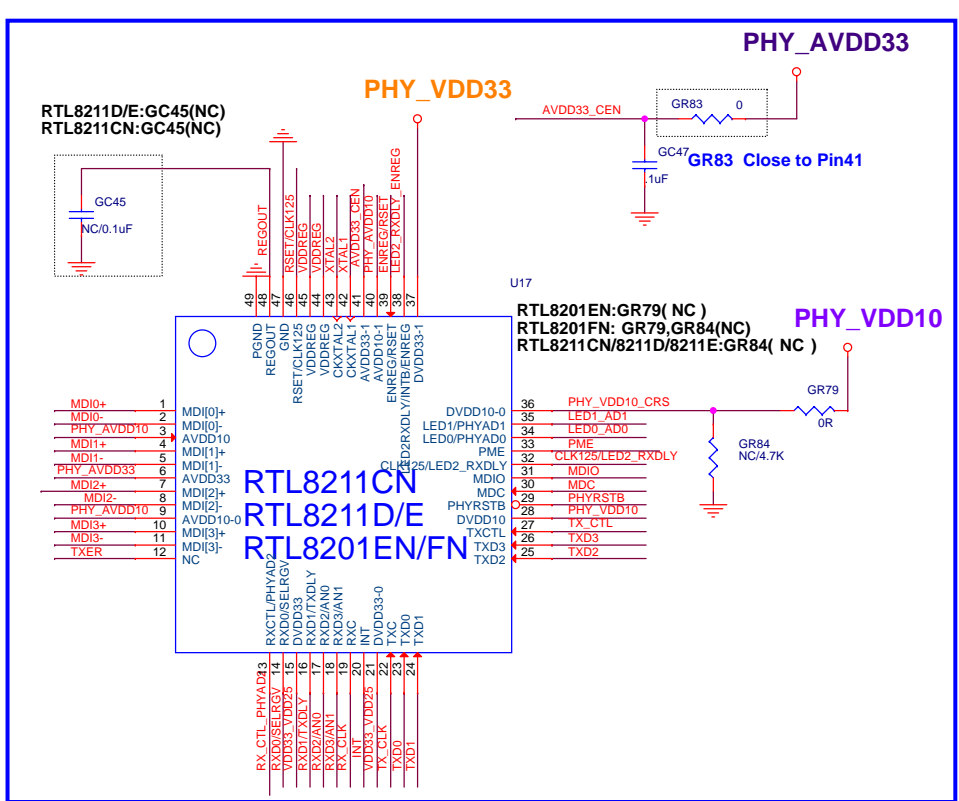
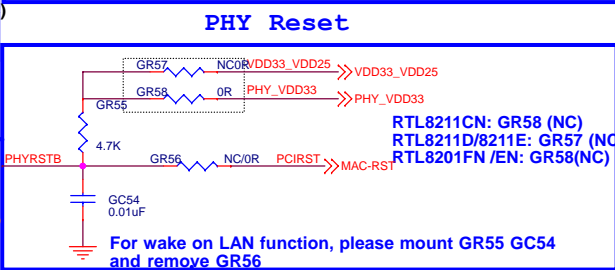
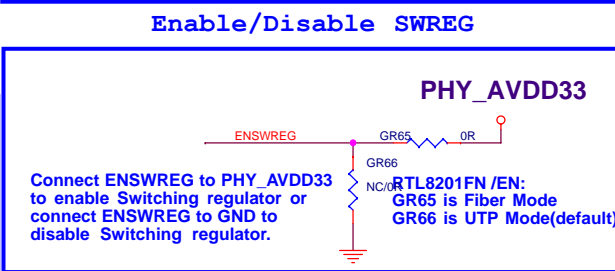
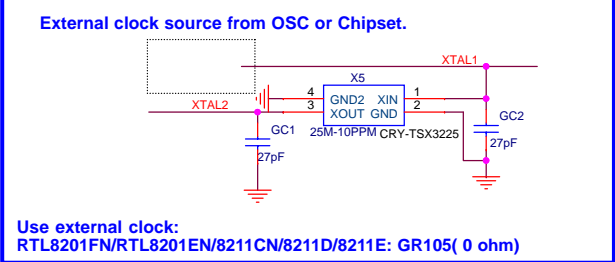
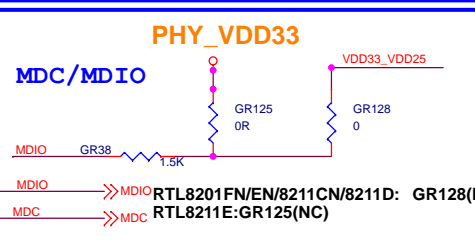
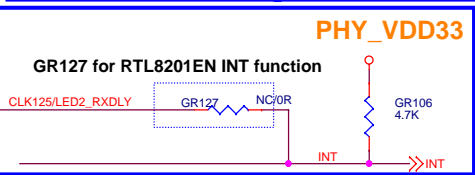
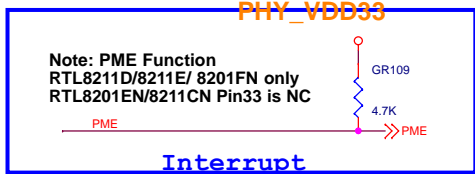


RTL8201FN/EN :
C40,C41,GL1 is NC
GC33,GC38,GC35,GC37 is NC

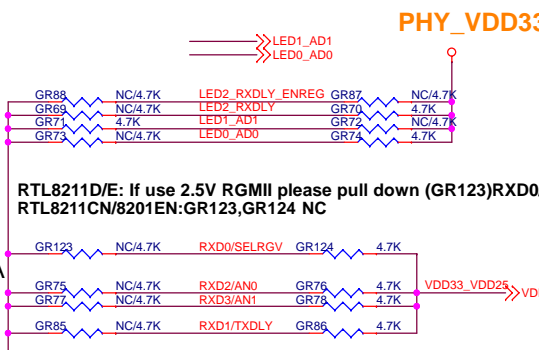
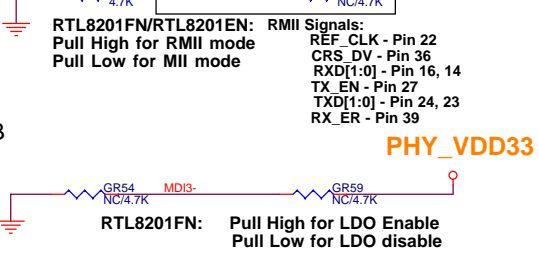
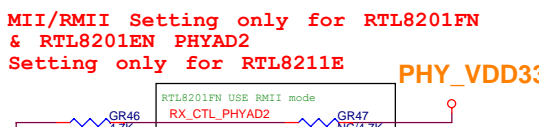
Reserve for EMI



PINE64			
Title SOPINE Baseboard " Model A"			
Size A3	Document Number	EMAC/GMAC	Rev 0.9
Date:	Sheet 18 of 19		



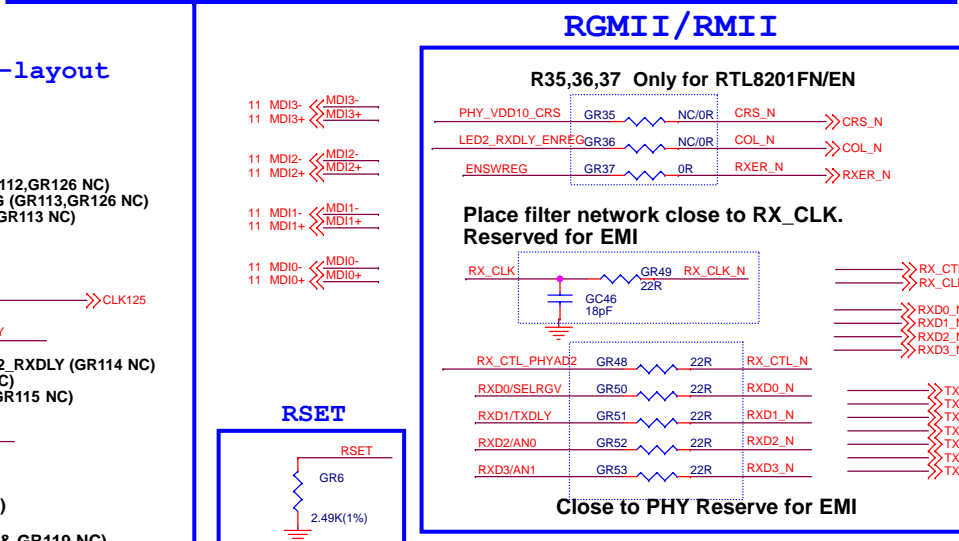
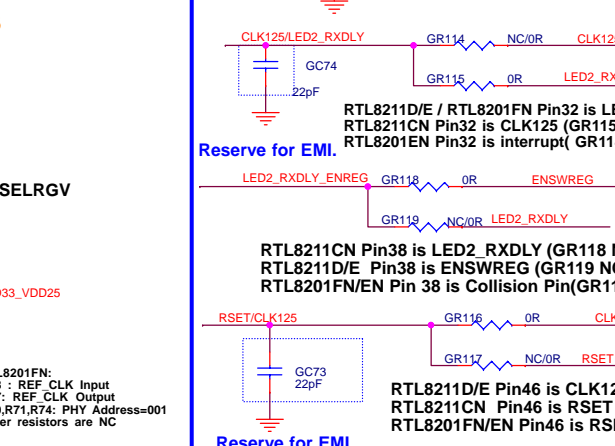
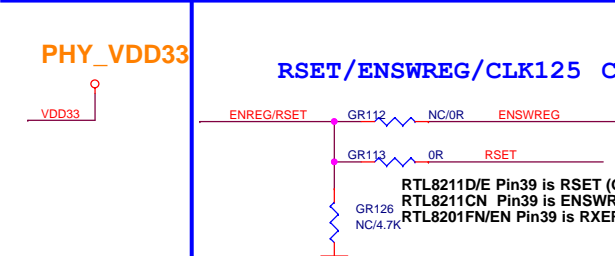
Configuration Setting



RTL8211CN/8211D/8211E:
GR76,GR78: Config for all capability
GR71,GR74: PHY Address=01 (8211D/8211CN)
GR46,GR71,R74: PHY Address=001 (8211E)
GR69,GR85: Without TX/RX Delay

RTL8201EN:
GR88:MII Interface
GR87:SNII Interface
GR71,GR74: PHY Address=001
Other resistors are NC

RTL8201FN:
R78 : REF CLK Input
R77: REF CLK Output
R69,R71,R74: PHY Address=001
Other resistors are NC



PINE64

Title				SOPINE Baseboard " Model A"		
Size	A3	Document Number	EMAC / GMAC		Rev	0.9
Date:		Sheet	19	of	19	